IN THE CLAIMS:

Claim 1 (Once Amended):

1. For use in a data processing system having an instruction processor to execute instructions included in the instruction set of the instruction processor, the instruction processor having an instruction pipeline capable of initiating simultaneous execution on a variable number of the instructions in a predetermined period of time, a system for programmably controlling the variable number of the instructions beginning execution within the instruction pipeline during the predetermined period of time, comprising:

a first storage device to receive and to store a programmable count value indicative of a predetermined number of instructions; and

a logic sequencer coupled to said first storage device to receive said programmable count value, and in response thereto, to generate a pipeline control signal provided to the instruction pipeline to cause the instruction pipeline to receive, and to initiate concurrent execution on, [a] the predetermined number of the instructions in the predetermined period of time [as determined by said programmable count value].

Claim 11: (Once Amended):

11. For use in an instruction pipeline of an instruction processor, the instruction processor to execute instructions that are part of the instruction set of the instruction processor, the instruction pipeline being adapted to initiate the execution of a variable number of instructions, up to a predetermined maximum number of instructions, within a predetermined period of time when the instruction pipeline is operating in a default mode, and whereby up to said predetermined maximum number of instructions may be executing simultaneously within the instruction pipeline, the instruction pipeline including a pipeline controller to generate a pipeline control signal for temporarily preventing ones of the instructions from entering the instruction pipeline, a method of utilizing the pipeline [depth] controller to control the number of instructions for which execution is initiated by the instruction pipeline within the predetermined period of time, comprising the steps:

providing a count to the pipeline [depth] controller; and

utilizing the pipeline [depth] controller to selectively assert the pipeline control signal to cause the instruction pipeline to initiate the execution of the number of instructions specified by said count within a period of time equal to the predetermined period of time.

Claim 12 (Once Amended):

12. The method of Claim 11, wherein the pipeline [depth] controller includes a programmable enable circuit to selectively enable the generation of the pipeline control signal, and further including the step of:

programming the programmable enable circuit to enable the pipeline [depth] controller to repeatedly selectively assert the pipeline control signal such that the instruction pipeline initiates the execution of the number of instructions specified by said count during successive periods of time that are each equal to the predetermined period of time.

Claim 13 (Once Amended):

13. The method of Claim 11, wherein the instruction processor includes a first memory device coupled to the pipeline [depth] controller, and further including the steps of:

storing within the first memory device respective first count signals for each of first predetermined ones of the instructions; and

providing said respective first count signals to the pipeline controller as said count when a respective one of said first predetermined ones of the instructions enters the instruction pipeline.

Claim 14 (Once Amended):

14. The method of Claim 13, wherein the pipeline [depth] controller may be programmably enabled, and further including the step of:

enabling the pipeline controller to be responsive to said respective first count signals.

Claim 15 (Once Amended):

15. The method of Claim 13, wherein the instruction processor includes a second memory device coupled to the pipeline [depth] controller, and further including the steps of:

storing within the first memory device respective first compare signals for each of said first predetermined ones of the instructions;

storing within the second memory device respective second compare signals for each of second predetermined ones of the instructions; and

comparing said respective first compare signals for an instruction N+1 that is one of said first predetermined ones of the instructions and that is executing within the instruction pipeline to said respective second compare signals for an instruction N that is one of said second predetermined ones of the instructions, and that entered the instruction pipeline for execution before said instruction N+1 entered the instruction pipeline, said comparing step performed to determine whether a predetermined relationship exists between said respective first compare signals for said instruction N+1 and said respective second compare signals for said instruction N;

and wherein said step of providing said respective first count signals to the pipeline controller is performed only if said predetermined relationship exists.

Claim 18 (Once Amended):

18. The method of Claim 15, wherein the second memory device further stores respective second count signals for each of said second predetermined ones of the instructions, and wherein said step of providing said first respective count signals to the pipeline [depth] controller includes the step of selecting whether said respective second count signals will be substituted for use as said count instead of said first respective count signals.